Express Mail Number EV364033438US PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of James Thomas Doyle et al. Application No. New (Div. of 10/272,035) Filed: Herewith For: MOS TRANSISTOR WITH SERRATED GATE STRUCTURES (as amended)	Group Art Unit: Unknown Examiner: Unknown INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith information of which applicants are aware, which applicants believe may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

This Information Disclosure Statement:

(a) [X] accompanies the new patent application submitted herewith. 37 CFR § 1.97(a).

(b) [ ] is filed within three months after the filing date of the application or within three months after the date of entry of the national stage of a PCT application as set forth in 37 CFR § 1.491.

(c) [ ] as far as is known to the undersigned, is filed before the mailing date of a first Office Action on the merits.

(d) [ ] is filed after the first office action and more than three months after the application's filing date or PCT national stage date of entry filing but, as far as is known to the undersigned, prior to the mailing date of either a final rejection or a notice of allowance, whichever occurs first, and is accompanied by either the fee ($180) set forth in 37 CFR § 1.17(p) or a certification as specified in 37 CFR § 1.97(e), as checked below.

(e) [ ] is filed after the mailing date of either a final rejection or a notice of allowance, whichever occurred first, and is accompanied by the fee ($180) set forth in 37 CFR § 1.17(i)(1) and a certification as specified in 37 CFR § 1.97(e), as checked below. This document is to be considered as a petition requesting consideration of the information disclosure statement.

[If either of boxes (d) or (e) are checked above, the following "certification" under 37 CFR § 1.97(e) may need to be completed.] The undersigned certifies that:

(f) [ ] Each item of information contained in the information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

(g) [ ] No item of information contained in this information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this information disclosure statement.

A list of the patent(s) or publications(s) is set forth on the attached Form PTO-1449 (Modified). A copy of the items on PTO-1449 (Modified) is supplied herewith:

(h) [ ] each

(i) [X] none

(j) [ ] only those listed below:

Those patent(s) or publication(s) which are marked with an asterisk (*) in the attached form PTO-1449 (Modified) are not supplied because they:

[X] were previously cited by or submitted to the Office in a prior application no. 10/272,035 filed October 15, 2002 and relied upon in this application for an earlier filing date under 35 U.S.C. § 120 or

[ ] are hereby waived pursuant to 37 CFR 1.98 (a)(2)(i) for all U.S. national patent applications filed after June 30, 2003.

A concise explanation of relevance of the described above and attached information is:

(k) [X] not given

(l) [ ] given for each listed item

(m) [ ] given for only non-English language listed item(s) [Required]

(n) [ ] is in the form of an English language copy of a Search Report from a foreign patent office, issued in a counterpart application, which refers to the relevant portions of the references [copy attached].

While the information disclosed in this Information Disclosure Statement may be "material" pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that the information referred to is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR § 1.56(a) exists. It is submitted that the Information Disclosure Statement is in compliance with 37 CFR § 1.98 and MPEP § 609 and the Examiner is respectfully requested to consider the above-described and attached information.

Respectfully submitted,

Dated: 4-14-04

By: _____
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Atty. Docket No: 100-19410 (P05247-D01)

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FORM PTO-1449 **INFORMATION DISCLOSURE CITATION IN AN APPLICATION** *(Use several sheets if necessary)* Express Mail Number EV340334385	Docket Number (Optional) 100-19410 (P05247-D01)	Application No. New (Div. of 10/272,035)
	Applicant(s) James Thomas Doyle et al.	
	Filing Date Herewith	Group Art Unit Unknown

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*	
	*Dragan Maksimovic, Bruno Kranzen, Sandeep Dhar and Ravindra Ambatipudi, U.S. Patent Application No. 10/053,226, filed January 19, 2002, entitled "An Adaptive Voltage Scaling Digital Processing Component and Method of Operating the Same".
	*Bruno Kranzen and Dragan Maksimovic, U.S. Patent Application No. 10/053,227, filed January 19, 2002, entitled "Adaptive Voltage Scaling Clock Generator for Use in a Digital Processing Component and Method of Operating the Same".
	*Dragan Maksimovic and Sandeep Dhar, U.S. Patent Application No. 10/053,828, filed January 19, 2002, entitled "System for Adjusting a Power Supply Level of a Digital Processing Component and Method of Operating the Same".
	*Dragan Maksimovic, Ravindra Ambatipudi, Sandeep Dhar and Bruno Krazen, U.S. Patent Application No. 10/053,228, filed January 19, 2002, entitled "An Adaptive Voltage Scaling Power Supply for Use in a Digital Processing Component and Method of Operating the Same".
	*James T. Doyle and Dragan Maksimovic, U.S. Patent Application No. 10/160,428, filed March 26, 2002, entitled "Method and System for Minimizing Power Consumption in Mobile Devices Using Cooperative Adaptive Voltage and Threshold Scaling".
	*Dragan Maksimovic and James Thomas Doyle, U.S. Patent Application No. 10/166,822, filed June 10, 2002, entitled "Serial Digital Communication Superimposed on a Digital Signal Over a Single Wire".
	*Dragan Maksimovic and Sandeep Dhar, U.S. Patent Application No. 10/236,482, filed September 6, 2002, entitled "Method and System for Providing Self-Calibration for Adaptively Adjusting a Power Supply Voltage in a Digital Processing System".
	*Mark F. Rives, U.S. Patent Application No. 10/246,971, filed September 19, 2002, entitled "Power Supply System and Method that Utilizes an Open Loop Power Supply Control".
	*Jim Doyle and Bill Broach, Small Gains in Power Efficiency Now, Bigger Gains Tomorrow [online]. July 9, 2002 [retrieved on 2003-02-01]. Retrieved from the Internet: <URL: http://www.commsdesign.com/design_corner/OEG20020709S0022>. pps. 1-5.
	*Robert W. Erickson and Dragan Maksimovic, Fundamentals of Power Electronics, Second Edition, Kluwer Academic Publishers, 2001, pp. 333.
	*Krisztian Flautner, Steven Reinhardt and Trevor Mudge, Automatic Performance Setting for Dynamic Voltage Scaling, Wireless Networks, Volume 8, Issue 5, September 2002, pps. 507-520, and Citation, pps. 1-3, [online]. [retrieved on 2003-02-02]. Retrieved from the Internet: <URL: http://portal.acm.org/citation.cfm?id=582455.582463&coll=portal&dl=ACM&idx=J804&p....>.
	*Krisztian Flautner, Steven Reinhardt and Trevor Mudge, Automatic Performance Setting for Dynamic Voltage Scaling [online]. May 30, 2001, [retrieved on 2003-02-02]. Retrieved from the Internet: <URL: http://www.eecs.umich.edu/~tnm/papers/mobicom01.pdf>. pps. 1-12.
	*Texas Instruments, "Synchronous-Buck PWM Controller With NMOS LDO Controller", TPS5110, SLVS025A-April 2002, Revised June 2002.
	*Joonho Gil, Minkyu Je, Jongho Lee and Hyungcheol Shin, "A High Speed and Low Power SOI Inverter Using Active Body-Bias", Association of Computing Machinery, ISLPED98, Monterey, CA, 1998, pps. 59-63.
	*Oliver Weinfurtner, "Switcher Output Stages on Neptune 28 (CMOS7-5), Neptune 28 Output Stage Results, September 24, 2001, pps. 1-8.
	*Intel XScale Core, Developer's Manual, December 2000, [online], [retrieved on 2003-02-02]. Retrieved from the Internet: <URL: http://developer.intel.com/design/intelxscale/27347301.pdf>. pps. 1-1 through B-1.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.